



P61089B

Dual Programmable Thyristor Transient Voltage Suppressor

版本号
202207-A

Description

This device has been especially designed to protect 2 new high voltage, as well as classical SLICs, against transient overvoltages. Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to $-V_{BAT}$ through the gate. This component presents a very low gate triggering current in order to reduce the current consumption on printed circuit board the firing phase. This devices are not subject to aging and provide a fail safe mode in short circuit for a better protection. Pic 1 and pic 2 are the device symbol and the package.

Features and Benefits

- Dual Voltage-Tracking Protectors
- wide negative pressure range: $V_{MGL} = -167V_{MAX}$
- low dynamic switching voltage: V_{FP} and V_{DGL}
- low gate triggering current : $I_{GT} = 6mA_{Max}$
- Peak Pulse Current: $I_{PP} = 50A$ (10/700 μ s)
- high Holding current : $I_H \geq 50mA$

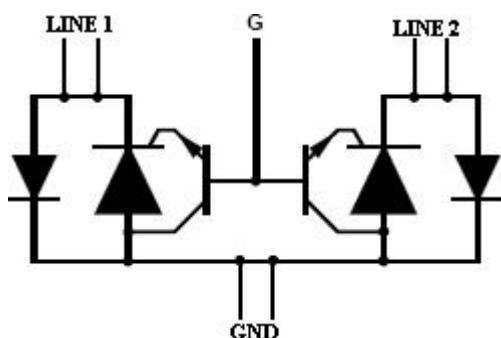
Application field

P61089B are designed to protect communication equipment such as SPC exchanger from damaging overvoltage transients in the second level.

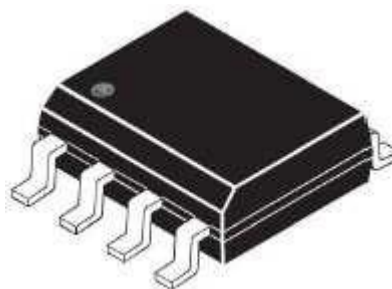
Characteristic parameters

symbo l	Rated value	unit
V_{MGL}	-167	V
$I_{PP}(10/700\mu s)$	50	A
I_H	50	mA

Package :SOP-8



Pic.1 Device equivalent structure



Pic.2 Device type SOP-8



Electrical Parameters

Standard

type	Wave shape		ITSP
ITU-T K.20/21and K.45	voltage	10/700 μ s	50A
	current	5/310 μ s	

Electrical characteristics

- Absolute maximum ratings $T = 25^{\circ}\text{C}$ unless otherwise noted^a

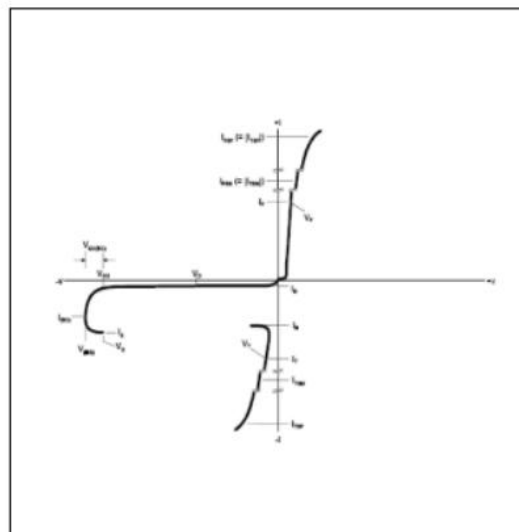
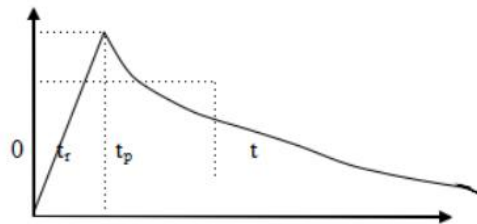
symbol	parameters	value	unit
V_{PP}/I_{PP}	Peak pulse voltage /current (tip.1)	10/700 μ s	2000
		5/310 μ s	50
I_{TSM}	Non repetitive peak pulse Current(F=60Hz)	$t_p=500\text{ms}$	6.5
		$t=1\text{s}$	4.6
I_{GSM}	Maximum gate current (half sinusoid $t_p=10\text{ms}$)	2	A
V_{MLG}	Line-ground maximum voltage	-170	V
V_{MGL}	Gate-line maximum voltage	-167	V
T_{stg}	Storage Temperature Range	-55~150	$^{\circ}\text{C}$
T_j	maximum temperature	150	$^{\circ}\text{C}$
T_L	maximum sustainable temperature of solder in 10 seconds	260	$^{\circ}\text{C}$

tip.1: pulse form:

5/310 μ s $t_r=5\mu$ s $t_p=310\mu$ s 100% I_{PP}

- V-I characteristic curve ($T = 25^{\circ}\text{C}$)^a

symbol	parameters
I_{GT}	Gate trigger current
I_H	Holding current
I_{RM}	Line-ground reverse leakage current
I_{RG}	Gate-line reverse leakage current
V_{RM}	Line-ground reverse voltage
V_F	Line-ground voltage
V_{GT}	gate trigger voltage
V_{FP}	Line-ground peak voltage
V_{DGL}	Gate-line dynamic switching voltage
V_{GATE}	Gate-ground voltage
V_{LG}	Line-ground voltage
C	Line-ground off state capacitance





Electrical Parameters

Absolute maximum ratings $T_a = 25^\circ\text{C}$ unless otherwise noted

● Line-ground diode parameters

symbol	Test conditions	Max.	unit
V_F	$I_F=5\text{A}$, $t_p=500\mu\text{s}$	3	V
V_{FP}	10/700 μs 1.5kV $R_P=10\Omega$ (tip. 1)	5	V

tip.1 $\diamond V_{FP}$ refers to test circuit 2, R_P is the protective resistance mounted on the card

● thyristor parameters($T_a=25^\circ\text{C}$)

symbol	Test conditions	Min.	Max.	unit
I_{GT}	$V_{GND}/LINE=-100\text{V}$	0.1	6	mA
I_H	$V_{GATE}=-100\text{V}$	50		mA
V_{GT}	Same to I_{GT}		2.5	V
I_{RG}	$T_C=25^\circ\text{C}$ $V_{RG}=-170\text{V}$		5	μA
	$T_C=70^\circ\text{C}$ $V_{RG}=-170\text{V}$		50	
V_{DGL}	$V_{GATE}=-100\text{V}$ (TIP.3) 10/700 μs 1.5kV $R_P=10\Omega$		10	V

Tip.2:see holding current (I_H)at test circuit 2;

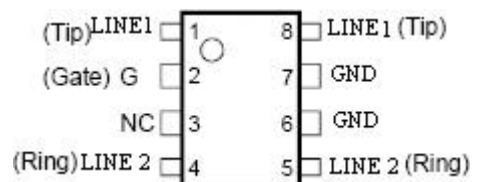
Tip.3:see V_{DGL} at test circuit 1, Don't make records if fluctuation time is less than 50ns.

● thyristor and diode parameters

Symbol	Test conditions	Max.	unit
I_{RM}	$T_C=25^\circ\text{C}$ $V_{GATE}/LINE=-1\text{V}$ $V_{RM}=-167$	5	μA
	$T_C=70^\circ\text{C}$ $V_{GATE}/LINE=-1\text{V}$ $V_{RM}=-167$	50	μA
C	$V_R=-3\text{V}$ $F=150\text{KHZ}$	100	pF
	$V_R=-48\text{V}$ $F=150\text{KHZ}$	50	pF

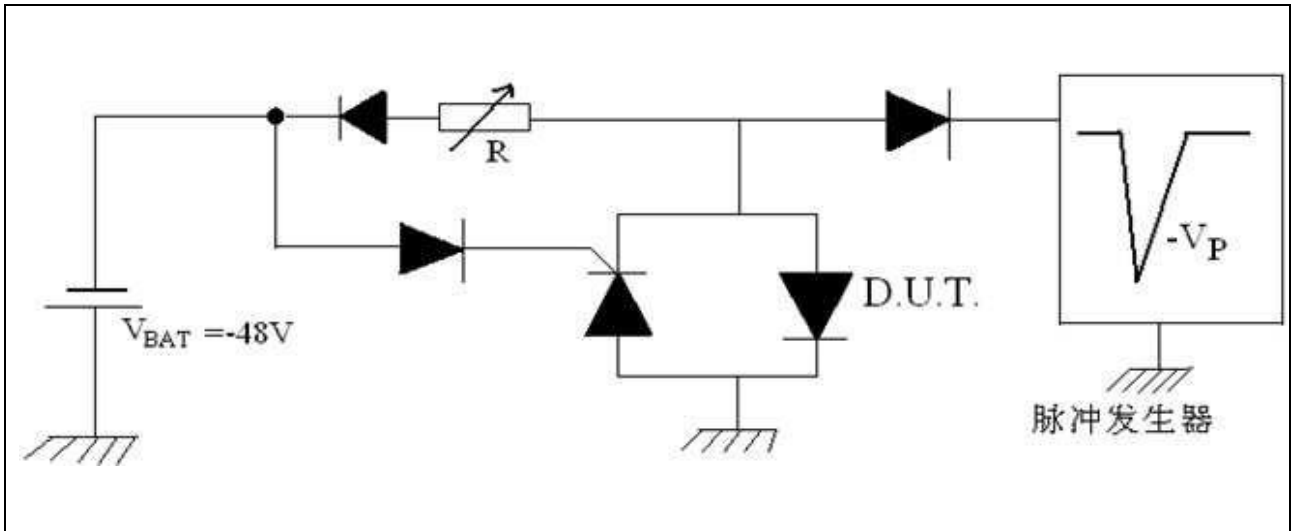
● Attention

For eliminate the overvoltage from the line
Parasitic induction,especially at the high speed
and short moment signal, we make
TIP and RING across the device.



■ Test method and circuit

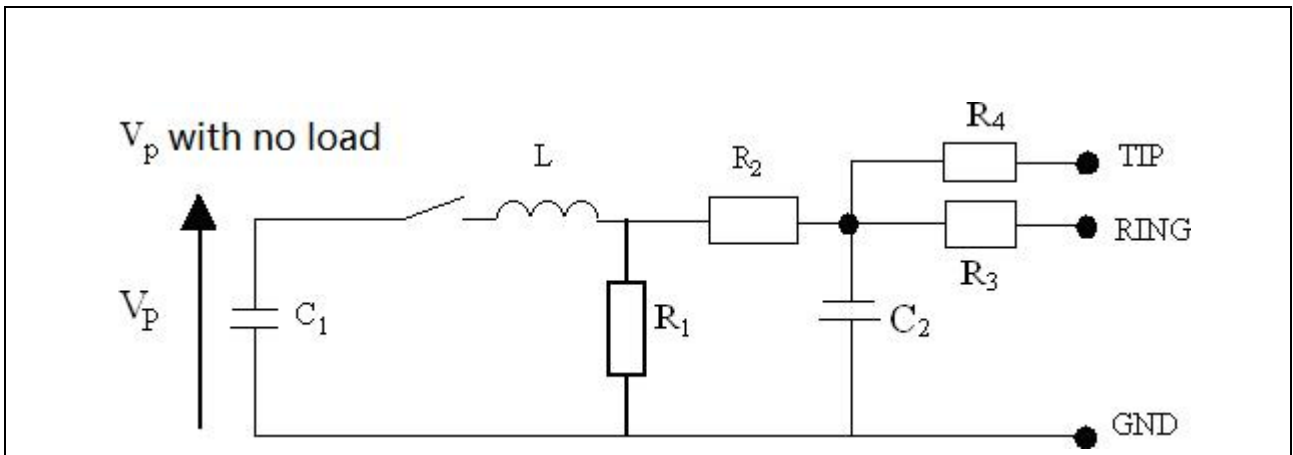
- Holding current test circuit(test circuit1)



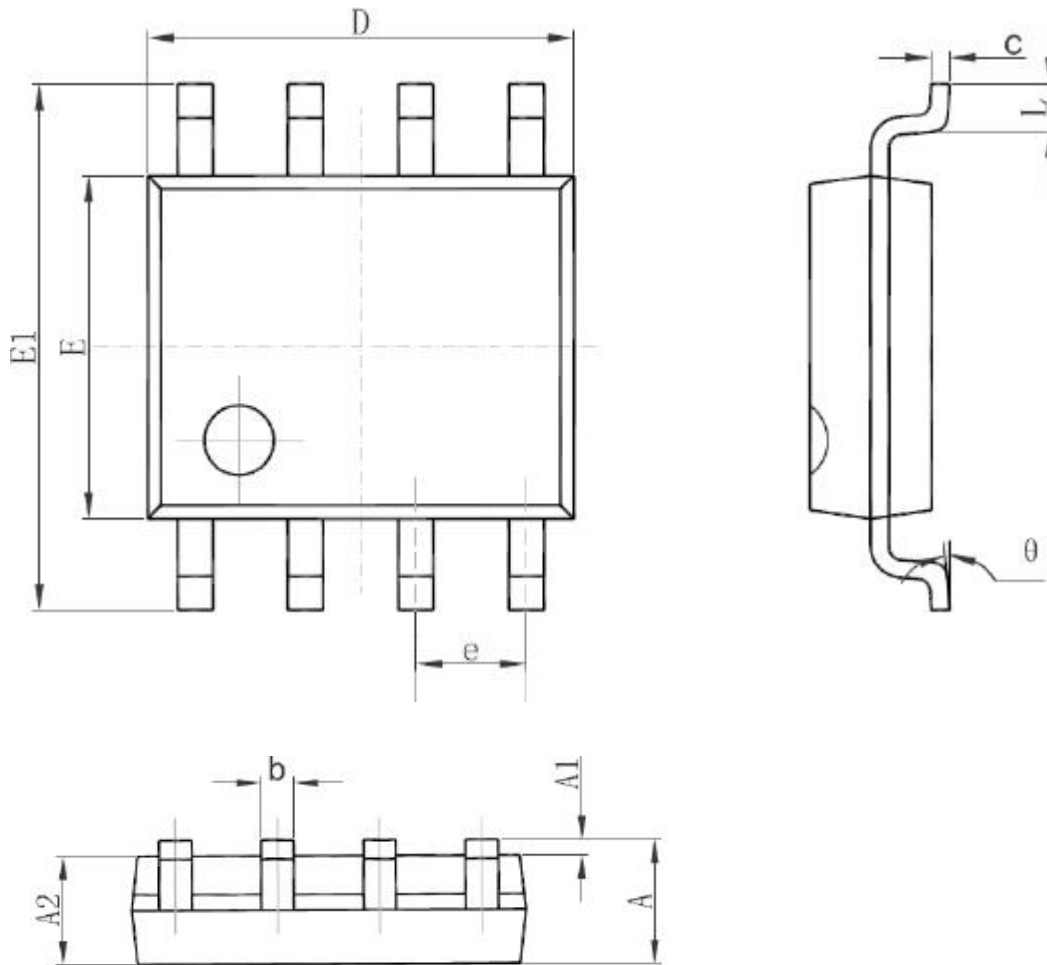
This is a “Conducting-cutoff” test. The test circuit can ascertain the size of holding current.

Test method :

- ① short out DUT , regulating current in I_H range;
 - ② set $I_{PP}=10A$, 10/1000 μs surge current triggers DUT;
 - ③ DUT must return to the off-state in 50ms. and
- V_{FP} and V_{DGL} test circuit2



Plue(us)		V_P (V)	C_1 (μF)	C_2 (μF)	L (μH)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	I_{PP} (A)	R_P (Ω)
t_r	t_p										
10	700	1500	20	200	0	50	15	25	25	30	10
1.2	50	1500	1	33	0	76	13	25	25	30	10
2	10	2500	10	0	1.1	1.3	0	3	3	38	62

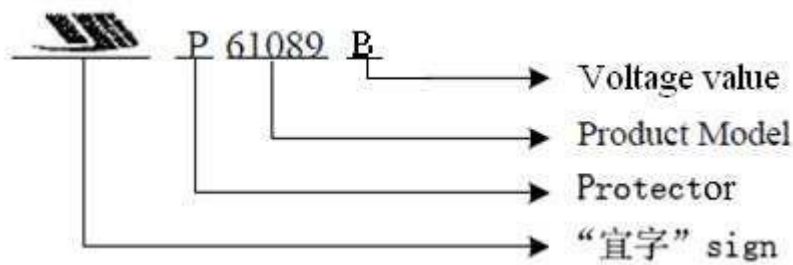
**Package size****■ Appearance size SOP-8**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking

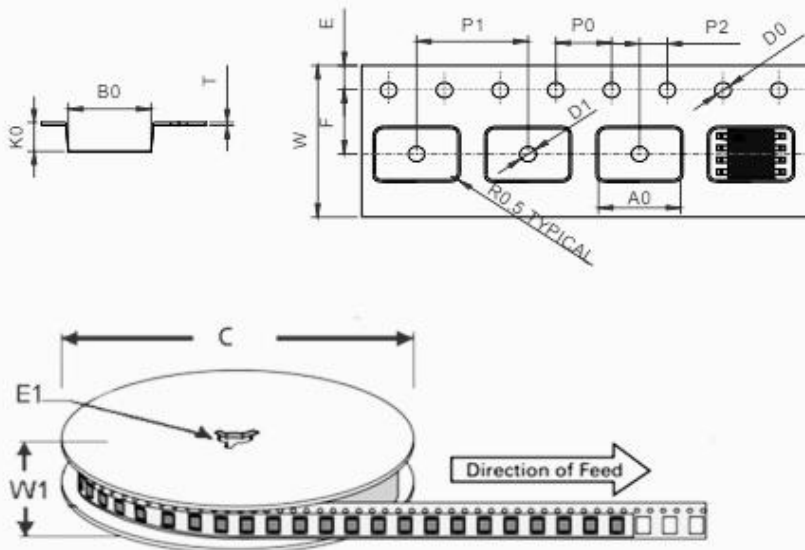


Naming Rule



XXYY:XX means year, YY means week.

Package Information



Ref.	Dimensions	
	Millimeters	Inches
A0	6.6±0.10	0.260 ± 0.004
B0	5.3±0.10	0.209 ± 0.004
C	330	13.0
D0	1.50±0.10	0.059 + 0.004
D1	1.50±0.10	0.059 + 0.004
E1	13.3±0.3	0.524± 0.012
E	1.75±0.1	0.069± 0.004
F	5.5±0.05	0.217 ± 0.002
K0	2.1±0.1	0.083 ± 0.004
P0	4.0±0.1	0.157± 0.004
P1	8.0±0.1	0.315± 0.004
P2	2.0±0.05	0.079 ± 0.002
T	0.24±0.1	0.009 ± 0.002
W	12.0±0.3	0.472 ± 0.012
W1	15.7±2.0	0.618 ± 0.079

Package Type	Quantity
SOP-8	4000



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